

HIGH SPEED SEMI-DYNAMIC FLIP-FLOP CIRCUIT

FIELD OF THE INVENTION

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The present invention relates generally to logic circuits and, more particularly, to semi-dynamic flip-flop circuits.

10 BACKGROUND OF THE INVENTION

FIG.1 shows a schematic diagram of one embodiment of a typical prior art semi-dynamic flip-flop circuit 100. As seen in FIG.1, semi-dynamic flip-flop circuit 100 included a first supply voltage 101, typically Vdd, a back-to-back inverter keeper circuit 103 and an NMOS stack 105 including NMOS transistors N1, N2 and N3, coupled to a second supply voltage 107, typically ground.

20 Semi-dynamic flip-flop circuit 100 had two modes, or phases, of operation; a pre-charge phase and an evaluation phase. In one embodiment of prior art semi-dynamic flip-flop circuit 100, in the pre-charge phase; the signal CLK 109 was low or a digital "0" and a first 25 node 190 was high, or a digital "1".

In the following discussion, assume that in the previous cycle, there was a path 191 from first node 190 to second supply voltage 107 through NMOS stack 105. In the evaluation phase, the signal CLK was high 30 or a digital "1", thereby providing first node 190 a path to second supply voltage 107.

Prior art semi-dynamic flip-flop circuit 100 functioned reasonably well in either low speed environments or low noise environments, however, semi-dynamic flip-flop circuit 100 did not perform well in 35 high speed and high noise applications. This was because, with prior art semi-dynamic flip-flop circuit

100, the transition from the pre-charge phase to the evaluation phase involved an inherent problem regarding first node 190, back-to-back inverter keeper circuit 103 and NMOS stack 105.

5 This problem arose because, in the pre-charge phase, at the transition from pre-charge to evaluation phase, the signal CLK goes to a digital "1" and NFET N1 is turned on, consequently, NMOS stack 105 provided a path 191 from first node 190 (FIG.1) to second supply voltage 107, typically ground, through NMOS stack 105. 10 Once path 191 was established, first node 190 should have dropped to a digital "0" as rapidly as possible to avoid delays in operation of prior art semi-dynamic flip-flop circuit 100. However, in this same time 15 frame, back-to-back inverter keeper circuit 103 was trying to hold first node 190 at first supply voltage 101, i.e., at a digital "1". Consequently, in semi-dynamic flip-flop circuit 100 there was an inherent "fight" between first node 190, trying to discharge to 20 "0" and back-to-back inverter keeper circuit 103 trying to hold first node 190 at "1" during the transition between pre-charge and evaluation. This fight resulted in a significant delay in the operation of prior art semi-dynamic flip-flop circuit 100.

25 To try and minimize this effect, i.e., the delay, resulting from the "fight" between first node 190, trying to discharge to "0" and back-to-back inverter keeper circuit 103 trying to hold first node 190 at "1" during the transition between pre-charge and 30 evaluation, a back-to-back inverter keeper circuit 103 with the smallest possible channel dimensions, i.e., the transistors making up back-to-back inverter keeper circuit 103 made intentionally small, could be employed. By this method, back-to-back inverter keeper 35 circuit 103 would hold node 190 high for as short a time as possible. In other words, back-to-back inverter keeper circuit 103 could be made weak and

small so it would lose its fight with first node 190 quickly. Unfortunately, this solution has significant drawbacks. In particular, by making back-to-back inverter keeper circuit 103 small, the noise immunity 5 of semi-dynamic flip-flop circuit 100 is compromised and this could lead to total failure of semi-dynamic flip-flop circuit 100 in high noise environments.

As a result of the situation discussed above, designers of semi-dynamic flip-flop circuit 100 were 10 constantly involved in a balancing act between minimizing the size and strength of back-to-back inverter keeper circuit 103, to increase speed of prior art semi-dynamic flip-flop circuit 100, and increasing the size and strength of back-to-back inverter keeper 15 circuit 103, to make semi-dynamic flip-flop circuit 100 more robust and noise immune. The result was that semi-dynamic flip-flop circuit 100 functioned reasonably well in either low speed environments or low noise environments, however, semi-dynamic flip-flop 20 circuit 100 did not perform well in high speed and high noise applications.

What is needed is a method and apparatus for creating an improved semi-dynamic flip-flop circuit that is capable of operation in both high speed and 25 high noise environments.

SUMMARY OF THE INVENTION

30 The present invention is directed to a method and apparatus for creating an improved semi-dynamic flip-flop circuit that is capable of operation in both high speed and high noise environments.

35 The high-speed semi-dynamic flip-flop circuit of the invention uses a keeper transistor to replace the back-to-back inverter keeper circuit of the prior art to avoid the fight between the first node and the prior

art back-to-back inverter keeper circuit described above.

According to the present invention, in operation, the high-speed semi-dynamic flip-flop circuit has two modes, or phases, of operation; a pre-charge phase and an evaluation phase. In one embodiment of a high-speed semi-dynamic flip-flop circuit of the invention, in the initial pre-charge phase, the CLK signal is low or a digital "0". Consequently, the output on a NAND gate 5 output is high. Consequently, a fourth transistor is in the on, or conducting state, and a second, or keeper, transistor of the invention is in the off, or non-conducting state.

In the evaluation phase, signal CLK is high or a digital "1" and the high speed semi-dynamic flip-flop circuit first node either remains high or it discharges depending on the data at a data input "d". If the high-speed semi-dynamic flip-flop circuit first node 15 discharges, the output of the NAND gate remains high and the fourth transistor remains on while the second transistor remains off. Consequently, there is no fight during the discharge process since the second transistor is off.

On the other hand, according to the present invention, if the data at data input "d" is low, this causes the high-speed semi-dynamic flip-flop circuit first node to remain high and the output at the NAND gate output switches to a low a predetermined number of 20 gate delays after the signal CLK. According to one embodiment of the present invention, this delay is provided by first and second inverters and ensures that the fourth transistor turns off and the second transistor turns on to reinforce a high on high speed semi-dynamic flip-flop circuit first node.

35 Since, according to the invention, the keeper transistor does not resist, compete or "fight" the discharge of the first node when there is a path from

the first node to the second supply voltage, circuit
designers are free to use larger and more powerful
second transistors. This, in turn, means that the
high-speed semi-dynamic flip-flop circuits of the
5 invention, in contrast to prior art semi-dynamic flip-
flop circuits, can be designed to have high noise
immunity and increased speed.

In addition, the modification of the invention is
space efficient and readily incorporated into existing
10 designs.

It is to be understood that both the foregoing
general description and following detailed description
are intended only to exemplify and explain the
invention as claimed.

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BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated
20 in, and constitute a part of this specification,
illustrate embodiments of the invention and, together
with the description, serve to explain the advantages
and principles of the invention. In the drawings:

25 FIG.1 shows a schematic diagram of a prior art
semi-dynamic flip-flop circuit; and

FIG.2 shows a schematic diagram of one embodiment
of a high-speed domino logic designed according to the
30 principles of the present invention.

DETAILED DESCRIPTION

35 The invention will now be described in reference
to the accompanying drawings. The same reference
numbers may be used throughout the drawings and the

following description to refer to the same or like parts.

5 The high-speed semi-dynamic flip-flop circuit of the invention (200 in FIG.2) uses a keeper, transistor (M2 in FIG.2) to replace the back-to-back inverter keeper circuit of the prior art (103 in FIG.1) to avoid the fight between the first node (290 in FIG.2) and the prior art back-to-back inverter keeper circuit described above.

10 According to the present invention, in operation, the high-speed semi-dynamic flip-flop circuit has two modes, or phases, of operation; a pre-charge phase and an evaluation phase. In one embodiment of a high-speed semi-dynamic flip-flop circuit of the invention, in the 15 initial pre-charge phase, the CLK signal (201 in FIG.2) is low or a digital "0". Consequently, the output on a NAND gate (217 in FIG.2) output (219 in FIG.2) is high and a fourth transistor (M4 in FIG.2) is in the on, or conducting state, and a second, or keeper, transistor 20 of the invention (M2 in FIG.2) is in the off, or non-conducting state.

25 In the evaluation phase, signal CLK is high or a digital "1" and the high speed semi-dynamic flip-flop circuit first node either remains high or it discharges depending on the data at a data input "d" (289 in FIG.2). If the high-speed semi-dynamic flip-flop circuit first node discharges, the output of the NAND gate remains high and the fourth transistor remains on while the second transistor remains off. Consequently, 30 there is no fight during the discharge process since the second transistor is off.

35 On the other hand, according to the present invention, if the data at data input "d" is low, this causes the high-speed semi-dynamic flip-flop circuit first node to remain high and the output at the NAND gate output switches to a low a predetermined number of gate delays after the signal CLK. According to one

embodiment of the present invention, this delay is provided by first and second inverters (205 and 209 in FIG.2) and ensures that the fourth transistor turns off and the second transistor turns on to reinforce a high 5 on high speed semi-dynamic flip-flop circuit first node.

Since, according to the invention, the keeper transistor does not resist, compete or "fight" the discharge of the first node when there is a path from 10 the first node to the second supply voltage, circuit designers are free to use larger and more powerful second transistors. This, in turn, means that the high-speed semi-dynamic flip-flop circuits of the invention, in contrast to prior art semi-dynamic flip- 15 flop circuits, can be designed to have high noise immunity and increased speed.

In addition, the modification of the invention is space efficient and readily incorporated into existing designs.

20 FIG.2 shows a schematic diagram of one embodiment of a high-speed semi-dynamic flip-flop circuit 200 of the invention. As seen in FIG.2, high speed semi-dynamic flip-flop circuit 200 includes a first supply voltage 204, in one embodiment Vdd, coupled to a first 25 flow electrode 253, of a first transistor M1; a first flow electrode 257 of a second transistor M2; and a first flow electrode 263 of a third transistor M3. The signal CLK 201 is coupled to a control electrode 251 of first transistor M1; a control electrode 295 of a sixth 30 transistor M6; a control electrode 271 of a seventh transistor M7; and an input 203 of a delay circuit 206 consisting, in one embodiment of a first inverter 205 and a second inverter 209.

According to one embodiment of the invention, a 35 second flow electrode 255 of first transistor M1 is coupled to a first node 290, also known as OUTBAR node 290. A second flow electrode 261 of second transistor

M2 is also coupled to first node 290. A control electrode 265 of third transistor M3 is coupled to first node 290 and a control electrode 277 of an eighth transistor M8. A second flow electrode 267 of third 5 transistor M3 is coupled to a high-speed semi-dynamic flip-flop circuit OUT terminal 229.

According to one embodiment of the invention, an output 207 of first inverter 205 is coupled to an input 208 of second inverter 209. An output 211 of second 10 inverter 209 is coupled to a first input 213 of NAND gate 217. A second input 215 of NAND gate 217 is coupled to first node 290. According to one embodiment of the invention, an output 219 of NAND gate 217 is coupled to a control electrode 259 of second transistor 15 M2 and a control electrode 221 of a fourth transistor M4.

According to one embodiment of the invention, first flow electrode 283 of fourth transistor M4 is coupled to first node 290. A second flow electrode 285 of fourth transistor M4 is coupled to a first flow electrode 287 of a fifth transistor M5. A second flow electrode 291 of fifth transistor M5 is coupled to a first flow electrode 293 of sixth transistor M6. A second flow electrode 297 of sixth transistor M6 is 20 coupled to a second supply voltage 202, in one embodiment ground. 25

According to one embodiment of the invention, a control electrode 289 of fifth transistor M5 is coupled to a data input "d" 289.

30 According to one embodiment of the invention, high-speed semi-dynamic flip-flop circuit OUT terminal 229 is coupled to a first flow electrode 269 of seventh transistor M7. A second flow electrode 273 of seventh transistor M7 is coupled to a first flow electrode 275 of eighth transistor M8. A second flow electrode 281 of eighth transistor M8 is coupled to second supply 35 voltage 202

According to one embodiment of the invention, high-speed semi-dynamic flip-flop circuit OUT terminal 229 is also coupled to an input 231 of third inverter 233. An output 235 of third inverter 233 is coupled to 5 a high-speed semi-dynamic flip-flop circuit qbar output 237.

According to one embodiment of the invention, high speed semi-dynamic flip-flop circuit OUT terminal 229 is also coupled to an input 224 of a fourth inverter 10 225 and output 228 of a fifth inverter 227. In addition, output 223 of fourth inverter 225 is coupled to input 222 of fifth inverter 227.

In one embodiment of the invention, first transistor M1, second transistor M2, and third 15 transistor M3 are PFET transistors and fourth transistor M4, fifth transistor M5, sixth transistor M6, seventh transistor M7, and eighth transistor M8 are NFET transistors. In this embodiment of the invention, first supply voltage 204 is Vdd and second supply 20 202 is ground. However, those of skill in the art will recognize that specific embodiments of high speed semi-dynamic flip-flop circuit 200 are shown in FIG.2 with specific transistors for illustrative 25 purposes only and that the NFETs and PFETS shown in the FIG.2 can be readily exchanged for PFETs and NFETs by reversing the polarities of the supply voltages 201 and 206 or by other well known circuit modifications.

In addition, those of skill in the art will readily recognize that the choice of first inverter 205 30 and second inverter 209 to comprise delay circuit 206 was made arbitrarily and for illustrative purposes only. Any number of inverters, or any form of delay circuitry could be easily used to accomplish the same result.

35 In operation, high-speed semi-dynamic flip-flop circuit 200 has two modes, or phases, of operation; a pre-charge phase and an evaluation phase. In one

embodiment of high-speed semi-dynamic flip-flop circuit 200, in the initial pre-charge phase, the signal CLK 201 is low or a digital "0". Consequently, the output on NAND gate output 219 is high and fourth transistor 5 M4 is in the on, or conducting state, and second transistor M2 is in the off, or non-conducting state.

In the evaluation phase, signal CLK is high or a digital "1" and high speed semi-dynamic flip-flop circuit first node 290 either remains high or it 10 discharges depending on the data at data input "d" 289. If high speed semi-dynamic flip-flop circuit first node 290 discharges, the output 219 of NAND gate 217 remains high and fourth transistor M4 remains on while second transistor M2 remains off. Consequently, there is no 15 fight during the discharge process since second transistor M2 is off.

On the other hand, if the data at data input "d" 289 is low, this causes high-speed semi-dynamic flip-flop circuit first node 290 to remain high and the 20 output at NAND gate output 219 switches to low three gate delays after the signal CLK 201. According to this one embodiment the present invention, this delay is provided by first and second inverters 205 and 209 and ensures that fourth transistor M4 turns off and 25 second transistor M2 turns on to reinforce a high on high speed semi-dynamic flip-flop circuit first node 290.

Those of skill in the art will recognize that the process discussed above will repeat for each switching 30 of the system clock. Those of skill in the art will further recognize that the choice of signal highs and signal lows was made arbitrarily for illustrative purposes only and that at other times, and in other embodiments of the invention, signal highs could be 35 replaced with signal lows and vice-versa.

According to the present invention, in addition to eliminating the fight to facilitate a faster discharge

of first node 190, the method and structure of the present invention increases the noise immunity of high-speed semi-dynamic flip-flop circuit 200 by allowing the size of second transistor M2 to be increased 5 without affecting circuit performance. This, in turn, means that the high-speed semi-dynamic flip-flop circuits 200, in contrast to prior art semi-dynamic flip-flop circuits, can be designed to have high noise immunity and increased speed.

10 As discussed above, the present invention is directed to a method and apparatus for creating a high-speed semi-dynamic flip-flop circuit that is capable of operation in both high speed and high noise environments.

15 Since, according to the invention, the second, or keeper, transistor does not resist, compete or "fight" the discharge of the first node when there is a path from the first node to the second supply voltage, circuit designers are free to use larger and more 20 powerful second transistors. This, in turn, means that the high-speed semi-dynamic flip-flop circuits of the invention, in contrast to prior art semi-dynamic flip-flop circuits, can be designed to have high noise immunity and increased speed.

25 The foregoing description of an implementation of the invention has been presented for purposes of illustration and description only, and therefore is not exhaustive and does not limit the invention to the precise form disclosed. Modifications and variations 30 are possible in light of the above teachings or may be acquired from practicing the invention.

For example, for illustrative purposes specific embodiments of the invention were shown with specific transistors. However, the NFETs and PFETs shown in the 35 figures can be readily exchanged for PFETs and NFETs by reversing the polarities of the supply voltages or by other well known circuit modifications.

In addition, those of skill in the art will readily recognize that the choice of first inverter 205 and second inverter 209 to comprise delay circuit 206 was made arbitrarily and for illustrative purposes 5 only. Any number of inverters, or any form of delay circuitry could be easily used to accomplish the same result.

Consequently, the scope of the invention is defined by the claims and their equivalents.